

<b>Notice of References Cited</b>	Application/Control No. 10/043,486	Applicant(s)/Patent Under Reexamination MOTIKA ET AL.	
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**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
<del>A</del>	A	US-5,303,246	04-1994	Anderson et al.	714/727
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
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	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

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	N					
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**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	"A Technique for Fault Diagnosis of Defects in Scan Chains", Guo et al., Int'l Test Conference Proceedings 2001, 30 Oct. - 1 Nov. 2001, pp 268-277.
	V	"Fast Technique for Locating Faults in Shift Register Latches", IBM Technical Bulletin NN7906229, June, 1979.
	W	"Combined Multi Corner Testing with Time and or Voltage Modulation", IBM Technical Bulletin NN81081677, August 1981.
	X	"Measurement of Power Bus Noise Sensitivity of VLSI Circuits with Automated Functional Tester", IBM Technical Disclosure NN9201226.

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.